EXYNO NANO CPU MODULE
DATASHEET

Eoxys Systems

Revision History		
Version	Date	Description of change
1.0	12-FEB-2022	Initial version
2.0	19-APR-2022	Corrected the pin mapping issues.

Table of Contents

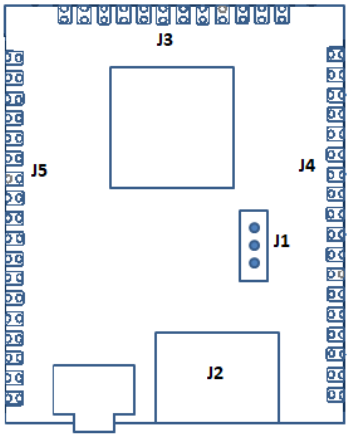
1 Overview

XENO+ Nano CPU Module can be used as core CPU module of any new IOT devices design of customers so that customers can focus only on adding sensors and power circuits around this CPU module for building their new IOT devices in short time.

The module has smallest possible size with STM32L4 series ARM Cortex-M4, 1MB Flash, 352KB/128KB RAM, UART/SPI/I2C ports and GPIOs. This module has USB Type C based 5V Power input with serial debug port and Battery power input options. This module has 3 pin SWD pins for SW development and SW debug via STM32CubeIDE for Embedded SW development for the device by the users.

2 CPU Module Overview

The below table shows the brief overview of modules:

	ENO-L100
Module Image	
Sensor Interface	UART, SPI, I2C, ADC, DAC, PWM and GPIOs
Pins	18x18 Castellated Pins on Left and Right side 12 Castellated Pins on Top side
Size in mm	55 x 35 mm

3 Product Features and Specifications

The XENO+ module product features and specifications are listed below:

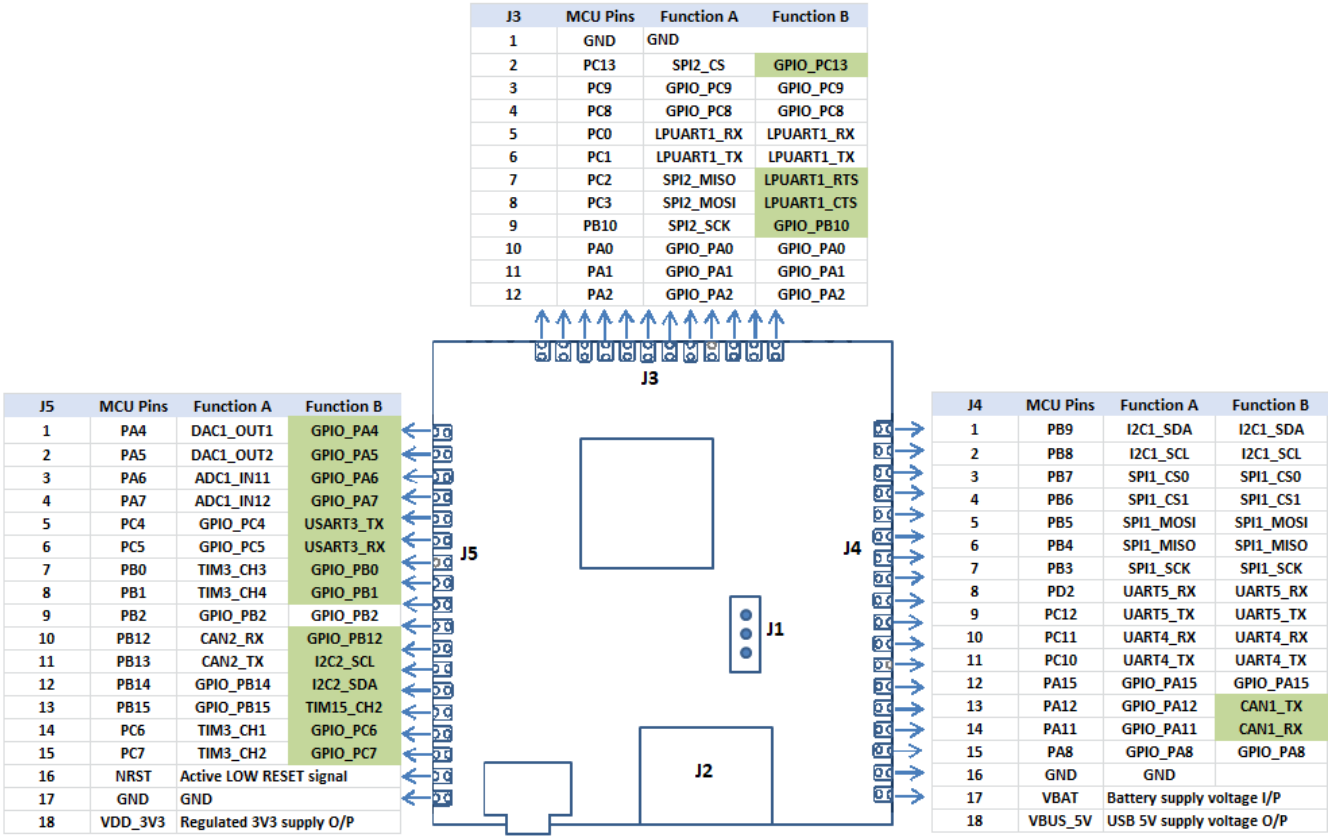
Table-1: The Product features and specifications

No.	Features	Specifications
Electro – Mechanical specification		
1	Boards Mounting	18x18 Castellated Pins
2	Wired interface	1x USB Type C for 5V Power and Serial debug UART interface for debug messages and user inputs.
.4	User SW programming	3 pin SWD pins for SW programming and debug via STM32CubeIDE
5	Operating temperature	-20 ~ + 85 ℃
6	Operating humidity	95% or less
7	Size	55x35 mm
8	Weight	5 grams

Power Specifications		
1	Module input voltage	5V from USB Type C connector * MOSFET based switch to auto cut-off battery power when USB 5V is present.
2	Battery input voltage	2.5V to 5V Battery power from non-rechargeable (or) re-chargeable battery. The battery options are listed below: * Two 1.5V AA Type Alkaline/Drycell non-rechargeable bat-teries connected in series for non-restricted transport. * 3.6V AA type (Li-SOCl2) non-rechargeable battery for Indus-trial applications. * 4.2V LiFePO4 18650rechargeable battery. The recharging circuit to be added in carrier board by customer.
CPU & Other Specifications		
1	CPU	STM32L4 series MCU with ARM Cortex-M4 at 80MHz
2	Flash Memory	1MB with Preassigned FOTA section
3	RAM	352KB/128KB SRAM
4	Sensor Interfaces	2x SPI 4x UART 2x I2C 2x CAN 2x ADC 2x DAC 4x PWM 19x GPIOs
5	RTOS	FreeRTOS

4 Module Pinouts:

This module has 18x18 Castellated pins. The Left side 18 pins mapping and Right side 18 pins mapping are listed below. The MCU port pins can be assigned with 2 predefined module func-tions: Function-A and Function-B. The users can also map custom functions as per STM32L4 na-tive GPIO functions on these pins.



J3	MCU Pins	Function A	Function B
1	GND	GND	
2	PC13	SPI2_CS	GPIO_PC13
3	PC9	GPIO_PC9	GPIO_PC9
4	PC8	GPIO_PC8	GPIO_PC8
5	PC0	LPUART1_RX	LPUART1_RX
6	PC1	LPUART1_TX	LPUART1_TX
7	PC2	SPI2_MISO	LPUART1_RTS
8	PC3	SPI2_MOSI	LPUART1_CTS
9	PB10	SPI2_SCK	GPIO_PB10
10	PA0	GPIO_PA0	GPIO_PA0
11	PA1	GPIO_PA1	GPIO_PA1
12	PA2	GPIO_PA2	GPIO_PA2

J5	MCU Pins	Function A	Function B
1	PA4	DAC1_OUT1	GPIO_PA4
2	PA5	DAC1_OUT2	GPIO_PA5
3	PA6	ADC1_IN11	GPIO_PA6
4	PA7	ADC1_IN12	GPIO_PA7
5	PC4	GPIO_PC4	USART3_TX
6	PC5	GPIO_PC5	USART3_RX
7	PB0	TIM3_CH3	GPIO_PB0
8	PB1	TIM3_CH4	GPIO_PB1
9	PB2	GPIO_PB2	GPIO_PB2
10	PB12	CAN2_RX	GPIO_PB12
11	PB13	CAN2_TX	I2C2_SCL
12	PB14	GPIO_PB14	I2C2_SDA
13	PB15	GPIO_PB15	TIM15_CH2
14	PC6	TIM3_CH1	GPIO_PC6
15	PC7	TIM3_CH2	GPIO_PC7
16	NRST	Active LOW RESET signal	
17	GND	GND	
18	VDD_3V3	Regulated 3V3 supply O/P	

J4	MCU Pins	Function A	Function B
1	PB9	I2C1_SDA	I2C1_SDA
2	PB8	I2C1_SCL	I2C1_SCL
3	PB7	SPI1_CS0	SPI1_CS0
4	PB6	SPI1_CS1	SPI1_CS1
5	PB5	SPI1_MOSI	SPI1_MOSI
6	PB4	SPI1_MISO	SPI1_MISO
7	PB3	SPI1_SCK	SPI1_SCK
8	PD2	UART5_RX	UART5_RX
9	PC12	UART5_TX	UART5_TX
10	PC11	UART4_RX	UART4_RX
11	PC10	UART4_TX	UART4_TX
12	PA15	GPIO_PA15	GPIO_PA15
13	PA12	GPIO_PA12	CAN1_TX
14	PA11	GPIO_PA11	CAN1_RX
15	PA8	GPIO_PA8	GPIO_PA8
16	GND	GND	
17	VBAT	Battery supply voltage I/P	
18	VBUS_5V	USB 5V supply voltage O/P	

4.1 Left side 18 pins connector signals

SNO	MCU Pins	Function A	Function B
1	PA4	DAC1_OUT1	GPIO_PA4
2	PA5	DAC1_OUT2	GPIO_PA5
3	PA6	ADC1_IN11	GPIO_PA6
4	PA7	ADC1_IN12	GPIO_PA7
5	PC4	GPIO_PC4	USART3_TX
6	PC5	GPIO_PC5	USART3_RX
7	PB0	TIM3_CH3	GPIO_PB0
8	PB1	TIM3_CH4	GPIO_PB1
9	PB2	GPIO_PB2	GPIO_PB2
10	PB12	CAN2_RX	GPIO_PB12
11	PB13	CAN2_TX	I2C2_SCL
12	PB14	GPIO_PB14	I2C2_SDA
13	PB15	GPIO_PB15	TIM15_CH2
14	PC6	TIM3_CH1	GPIO_PC6
15	PC7	TIM3_CH2	GPIO_PC7
16	NRST	Active LOW RESET signal to MCU. The Push button also asserts RESET signal to LOW.	
17	GND	GND pin of module.	

18	VDD_3V3	Regulated 3V3 supply output from module to other circuits of carrier board.

4.2 Right side 18 pins connector signals

SNO	MCU Pins	Function A	Function B
1	PB9	I2C1_SDA	I2C1_SDA
2	PB8	I2C1_SCL	I2C1_SCL
3	PB7	SPI1_CS0	SPI1_CS0
4	PB6	SPI1_CS1	SPI1_CS1
5	PB5	SPI1_MOSI	SPI1_MOSI
6	PB4	SPI1_MISO	SPI1_MISO
7	PB3	SPI1_SCK	SPI1_SCK
8	PD2	UART5_RX	UART5_RX
9	PC12	UART5_TX	UART5_TX
10	PC11	UART4_RX	UART4_RX
11	PC10	UART4_TX	UART4_TX
12	PA15	GPIO_PA15	GPIO_PA15
13	PA12	GPIO_PA12	CAN1_TX
14	PA11	GPIO_PA11	CAN1_RX
15	PA8	GPIO_PA8	GPIO_PA8
16	GND	GND pin of module	
17	VBAT	Battery supply voltage input to module with 3V to 6V range. If Battery is connected, the module works with this battery supply.	
18	VBUS_5V	USB 5V supply voltage output from module to other circuits of carrier board. This is USB 5V supply. When USB cable is removed, the module will switch to Battery supply on-the-fly, if battery is connected.	

4.3 Top side 12 pins connector signals

SNO	MCU Pins	Function A	Function B
1	GND	GND pin of module	
2	PC13	SPI2_CS	GPIO_PC13
3	PC9	GPIO_PC9	GPIO_PC9
4	PC8	GPIO_PC8	GPIO_PC8
5	PC0	LPUART1_RX	LPUART1_RX
6	PC1	LPUART1_TX	LPUART1_TX
7	PC2	SPI2_MISO	LPUART1_RTS
8	PC3	SPI2_MOSI	LPUART1_CTS
9	PB10	SPI2_SCK	GPIO_PB10
10	PA0	GPIO_PA0	GPIO_PA0
11	PA1	GPIO_PA1	GPIO_PA1
12	PA2	GPIO_PA2	GPIO_PA2

5 SW Functional Specifications

5.1 User Application Functional Specifications

This user application runs as main application which controls the sensors, interfaces, memory and data transfer of the IOT device. The network configuration, sensor configuration, sensor data transfer via TCP Sockets/HTTP/MQTT APIs are maintained by the user embedded application.

The embedded device's memory map is defined as per below table so that memory map has sections for FOTA Downloader, Actual user firmware and Backup user firmware.

Features	**Description**
Memory map of program flash of embedded device	1. **FOTA_DOWNLOADER_MEMORY** Contains ISR_VECTOR, FIRMWARE, USER_CONFIG, ACCESS_TOKEN memory segments. 2. **MAIN_FIRMWARE_MEMORY** Contains ISR_VECTOR and Main running app's MAIN_FIRMWARE, MAIN_FIRMWARE_SWVER info memory segments. 3. **BACKUP_FIRMWARE_MEMORY** Contains ISR_VECTOR and Main running app's BACKUP_FIRMWARE, BACKUP_FIRMWARE_SWVER info memory segments

After successful authentication of device, the server issues valid access token to the device. The access-token has a limited lifetime mentioned in minutes. When it expires the FOTA Downloader can fetch a new refresh-token. This access-token can be read by User Embedded application

available at below memory section: ACCESS_TOKEN memory segment. The user application keeps its firmware version name, SW version and release date in separate memory section: MAIN_FIRMWARE_SWVER info memory segment.

Features	Description

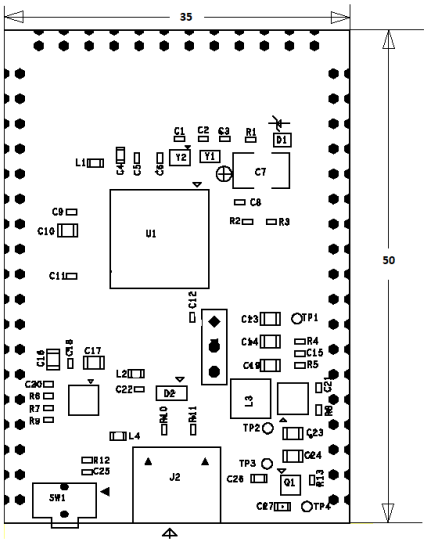
ACCESS_TOKEN memory segment: Access Token memory section	{
	ACCESS_TOKEN: <Access token>
	}

MAIN_FIRMWARE_SWVER memory segment: Main Firmware Info memory section (User application firmware info)	{
	FIRM_NAME: <Device-SW>
	SWVER: <V10>
	DATE: <dd-mon-yyyy>
	}

6 Module Layout and Dimensions

This module layout and dimensions are shown below.

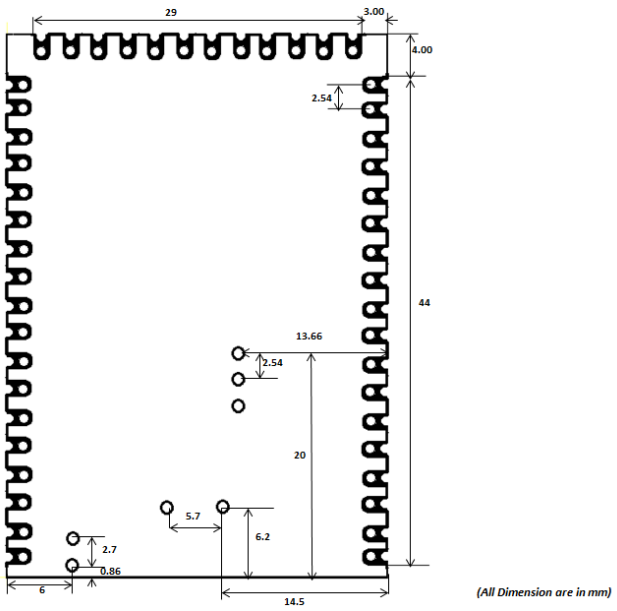
Module Dimensions (in mm)



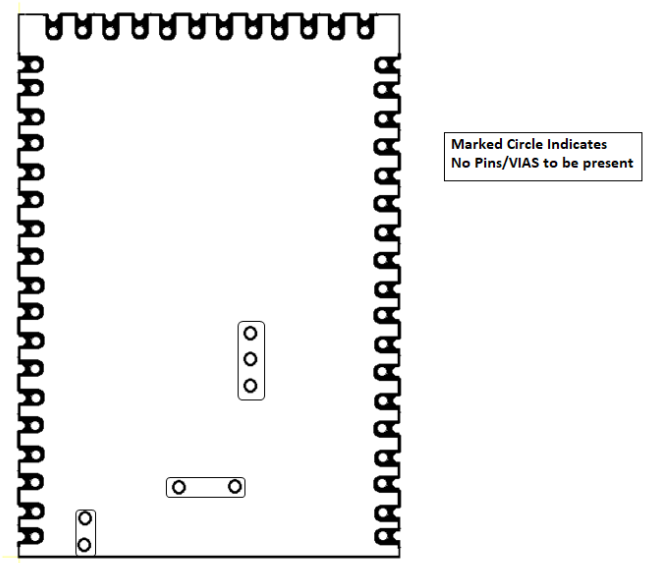
7 Mechanical Specifications

The XENO+ module is a single sided 55x35mm 1mm thick PCB with dual castellated/through-hole pins around the remaining edges. XENO+ module is designed to be usable as a surface mount module as well as being in Dual Inline Package (DIP) type format, with the 36 main user pins on a 2.54mm (0.1") pitch grid with 1mm holes.

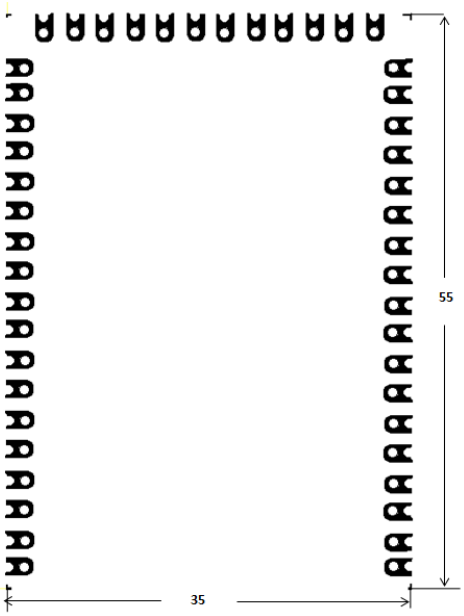
Mechanical Specifications



Mechanical Specifications with no pins/vias to be present



Carrier Board PCB Footprint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35